Technical Description

Radio Clock for IBM PC XT/AT and Compatible

6036

hopf Elektronik

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1 General Information about the Circuit Board 6036

- latest receiver design with faultless decoding of the signal even in difficult reception situations
- plugging jumpers not necessary! All address and mode settings are carried out by the software included in the delivery.
- access to various time information
- back-up clock function with maintenance free power supply
- TTL pulse output
- direct access to the milliseconds
- interrupt operation with freely programmable cyclic interruption in the range of 10 - 65536 milliseconds (ideal for testing purposes)
- DCF77 reception analysis function
- Operation as slave clock via synchronisation entry
- software for Windows NT ™
- option: serial interface RS232 [1]
- option: programmable protection for software producer (Dongle)
- option: software for NTP (Network Time Protocol) by TCP/IP

2 Starting the Radio Clock Circuit Board 6036

When installing the radio clock the computer and all the connected devices must be switched off.

Open the computer housing, plug the radio clock into a vacant extension space, connect the antenna and the clock is ready for operation.

The programme **"SERVICE.EXE"** serves to find the optimum antenna location and to check the clock function (see point 8).

(For further information about the software included in the delivery see *README.TXT*)

2.1 Hardware Setting Base Address and Mode

The board 6036 can operate with two different address types in the I/O range of the PC. Depending on the mode either

- Hex 10 (mode 6030-limited functions) or
- Hex 40 (mode 6035/6036)

memory can be addressed on the board.

[1] The description of the serial interface can be found on the supplied disk

State on delivery:

- mode 6036 (Hex 40 memory space)
- base address $280 (+$40=$2BF)
- jumper 2 connected

The address and mode can only be altered by means of the included service software **"SERVICE.EXE"** and not by means of jumpers.

It is absolutely necessary to disconnect jumper 2.

Connecting jumper J2 (see component mounting diagram in the appendix) turns the circuit board to the standard setting (address $280 mode 6035/6036).

SERVICE.EXE searches the I/O range for the clock board during the start. It is advisable to run the programme only under DOS, because hardware conflicts can cause system crashes.

Please note : A reset is necessary after changing the hardware address. The service software have to be started again.

2.1.1 Mode 6030 = Limited Address Range of Hex 10 Addresses

In this mode only time/date (CEST/CET and UTC) can be read out as BCD values. The other functions of the board like interrupt operation etc. are not available. Mode 6030 can only be left by reset of the board to the basic setting with jumper 2.

2.1.2 Mode 6035/6036 = Extended Address Range of Hex 40 Addresses

In this mode the radio clock board covers a range of Hex 40 addresses in the system. The board is delivered ex works in this configuration.

In mode 6035/6036 three different time information in two arithmetical formats are available.

2.1.3 UTC-Offset

The standard clock is delivered with a UTC-offset of -1 hour. This corresponds with the CET time zone. In countries outside this time zone the time offset must be changed if the UTC information is to be used. (Synchronisation of networks).

The SERVICE.EXE-program "set difference time" is used to carry out the alteration. Please note the following points:

- The offset is always the difference to the standard time. The summertime changeover is carried out automatically.
- East of the 0-meridian the entries have a -sign, those to the west have no sign or a +sign.

3 Organisation of the Internal Clock Data

The organisation of the interface is extremely simple. The data traffic to the radio clock is forwarded solely via the port addresses. The user has free access to the clock memory at all times. A handshake process to read out the data is not necessary.

To avoid errors the memory contents of the clock are not updated during an access from the PC. Permanent access to the clock board should therefore be avoided.

Available Information in Mode 6035/6036 and 6030

basic address (Hex)	content	format
+00	second	CET in BCD
+01	minute	CET in BCD
+02	hour	CET in BCD
+03	day	CET in BCD
+04	day of the week	CET in BCD (see 3.3)
+05	month	CET in BCD
+06	year	CET in BCD
+07	status	CET in BCD (see 4.)

Available Information in Mode 6035/6036

basic address (Hex)	content	format
+08 - 0F	clock data	CET binary

Available Information in Mode 6030

basic address (Hex)	content	format
+08 - 0F	clock data	UTC in BCD

Information Available in Mode 6035/6036 Only

basic address (Hex)	content	format
+10 - 17	clock data	UTC in BCD
+18 -1F	clock data	UTC binary
+20 - 27	clock data	CET in BCD
+28 - 2F	clock data	CET binary
+38 + 39	milliseconds	Low Byte (Intel Format)
	milliseconds	High Byte
+3B +3C	identification	High Byte = Hex 58
	identification	Low Byte = Hex 4E
	statistical value	**Can be called up as identification "clock installed?"**
+3D	DCF77 reception	in minutes (see 4.1)
+3D	key word	High Byte (Dongle)
+3F	key word	Low Byte (Dongle)

3.1 Example Reading of Time Data

CET binary from basic address (280 Hex) + offset 08 HEX

```
assembler :   mov dx,0288h   ; address second in dx register
              in al,dx       ; address in al register

pascal:       second := port [$288];

C,C++:        second = inp (0x288);
              second = inportb (0x288);
```

1. reading the seconds	CET binary from portaddress $288
2. reading the minutes	CET binary from portaddress $289
3. reading the hour	CET binary from portaddress $28A
4. reading the day	CET binary from portaddress $28B
5. reading the day of the week	CET binary from portaddress $28C
6. reading the month	CET binary from portaddress $28D
7. reading the year	CET binary from portaddress $28E
8. reading the status	CET binary from portaddress $28F

3.2 Data Format

The data format depends on the selected offset address. The status information is always given binarily and is to be decoded equally in all stated clocks. The value range of the day of the week is 1 - 7, Monday being 1.

3.3 Setting the Clock with a New Time (in mode 6035/6036 only)

Normally it is not necessary to use the set function in a radio clock. Time and date are read in by decoding the transmitter DCF77. Depending on the location it may be advantageous though to use this function.

The radio clock 6036 can be set with a new time. The time data are expected in the clock from offset 30h. The data format of the transmission is BCD only.

Basic address (280H) + offset address (30h) = Hex 2B0

Example Setting the Time 12:34:56 Wednesday the 23.04.90

No.	procedure	value(Hex)	portaddress (Hex)
1.	writing the seconds	56	2B0
2.	writing the minutes	34	2B1
3.	writing the hour	12	2B2
4.	writing the day of the week	03	2B3
5.	writing the day	23	2B4
6.	writing the month	04	2B5
7.	writing the year	90	2B6
8.	writing the status	40	2B7

Preconditions for a Valid Transmission:

- the data must be plausible
- the day of the week in the value range 01h-07h with 01h = Monday
- status word transmitted as Hex 40, 48 or 50

40 = without time zone bit
48 = Daylight-Time
50 = Standard-Time

3.4 Millisecond

The radio clock board also supply the millisecond. The millisecond is inserted as "word" in Intel format to the address "basic addr.+$38/ $39"

4 Status of the Clock and Reception Quality

The synchronisation status can be checked by means of the LEDs on the front panel. There are three LEDs with the following meaning:

- top LED: pulse LED flashes at second intervals for 100 or 200 ms, interrupts in the 59th second.
- middle LED: quartz operation
- bottom LED: radio operation

LED radio and quartz are lit = radio operation high precision

The microprocessor of the clock stores not only the time information in the memory but also the status of the clock or of the transmitter DCF77 rsp. Every time zone has its own status (see next table).

Available Information in the Clock Status:

- quartz operation
- radio operation
- radio operation controlled
- announcement of a leap second
- indication of winter time (WT)
- indication of summer time (ST)
- announcement of changeover from ST to WT rsp. from WT to ST

The status is transmitted binarily and is the same in all the clocks.

The individual Bits have the following Meaning:

bit7	**bit6**	**meaning (like LED radio and quartz)**
0	0	time invalid
0	1	quartz operation
1	0	radio operation
1	1	radio operation with controlled second edge

bit5 = 1	leap second - announcement
bit4 = 1	UTC + 1h (CET)
bit3 = 1	UTC + 2h (CEST)
bit2 = 1	announcement CET ⇔ CEST
bit1	no meaning at present
bit0	no meaning at present

Example: transmitted status HEX C8, binary 11001000

radio operation with control, summer time

4.1 Radio Operation

The time signal of the transmitter DCF77 must be received without any interference for at least three minutes to synchronise the radio clock board 6036. The completed synchronisation can be checked by the status LED or the status byte.

4.2 Quartz Operation

When the computer is started a built-in back up clock is read out. If the time is valid the board starts with the status **"quartz operation"**. If the back-up clock data are invalid the status is set to **"invalid"** and the internal time is set to 00 in all data positions.

The status **"quartz operation"** is also displayed when the reception of the DCF77-signal is disturbed, or if the transmitter is turned off due to thunderstorms etc. at the transmission location.

Please note : Status LED - quartz is lit.

4.3 Reception Quality and Control Accuracy

The number of **"good"** DCF77-data strings indicates the accuracy of the internal second marker of the clock processor.

A voltage controlled crystal oscillator of 12.288 MHz serves as time base for the quartz clock.

The second marker of the quartz clock is permanently compared with the well received second lowering of the DCF77-signal. From the deviation the computer produces a control value which adjusts the oscillator frequency to the accuracy of the DCF77 signal.

When synchronising the clock for the first time the time and the internal millisecond are taken over "hard". Afterwards a software control of the oscillator checks and controls the accuracy of the clock.

All control values are stored in a non-volatile memory so that after a voltage breakdown or a reset start values are immediately available to the processor.

Quality Counter and Control Accuracy

At the address **base address + Hex 3D** a reception quality counter is installed. On every minute change the synchronisation status is analysed and the quality counter increased by 1 if the DCF77-data string is valid. If the reception is disturbed the count moves down accordingly.

The counter runs from 0 to Hex FF (0 to 255 minutes). After a period of about 1 hour (first synchronisation) the accuracy of the quartz frequency has reached ± 2ppm.

5 Interrupt Possibilities

The board 6036 is equipped with multiple interrupt logic which make it possible to programme cyclic interrupt requests in the range of 1 to 65536 milliseconds .

When using this possibility, please take into consideration that the activation of an interrupt must be covered by an interrupt-service-routine (see demo programme **"IRQEXAMPL.PAS"**).

When using the interrupt possibilities of the radio clock board 6036 one of the following interrupt outputs must be activated by setting in the status byte.

The programme **IRQEXAMPL.PAS** on the disc included in the delivery activates the interrupt on line IRQ 3.

Available interrupt outputs : IRQ 2 to IRQ 7

Please note : Programming interrupt controlled software requires good knowledge of the operating system in the PC XT/AT. The delivered programme "**IRQEXAMPL.PAS**" is a simple example of how the interrupt is activated and cancelled under MS DOS.

5.1 Activation of the Interrupt Output (only in mode 6035/6036)

The interrupt is activated by the writing of a millisecond counter (two byte MSB, LSB) and a status byte (Hex 04) and the information which IRQ-line should be addressed. The start of the interrupt output is synchronised to the internal second change of the clock.

example:

interrupt every second = 1000 ms ⇨ MSB=Hex03, LSB=HexE8

on IRQ line 3

no.	process	value (hex)	port address (hex)
1	writing the milliseconds MSB	03	2B0
2	writing the milliseconds LSB	E8	2B1
3	writing the IRQ number	03	2B2
4	writing the start command	04	2B7

5.2 Secondsynchronous Interrupts

In contrast to the above described interrupt handling, the interrupt can be executed synchronised on the internal second.

The advantage to the strictly cyclic IRQ is, that in case of a bad reception situation the clock activates an IRQ on every second-, minute- or hour-change.

Additionally a constant delay-value (0-999 milliseconds) can be used to delay the interrupt output.

Second-, minute and hour-IRQs can be generated.

start command : 05 = second interrupt
06 = minute interrupt
07 = hour interrupt

Example: activate an interrupt, every minute, 100 ms after the minute-change.

no:	process	value (hex)	portadress (hex)
1.	writing the milliseconds MSB	00	2B0
2.	writing the milliseconds LSB	64	2B1
3.	writing the IRQ number	03	2B2
4.	writing start command	06	2B7

5.3 Stopping the Interrupt Output

The interrupt is deactivated by writing a status byte (Hex 02).

no.	process	value (hex)	port address (hex)
1.	writing the stop command	02	2B7

6 Reset of the Clock (only in Mode 6035/6036)

The clock can initialise itself if the according status byte is sent. The reset is caused by writing the status byte (Hex 01).

no.	process	value (hex)	port address (hex)
1.	writing the reset command	01	2B7

7 Master / Slave Operation of the Clock (in mode 6035/6036 only)

The clock can change between master and slave operation if the according statusbyte is sent. This mechanism can realise clock chains which run on one antenna. The adjustment is possible in mode 6035/6036 only.

The first clock becomes the master and receives the signal from the antenna. This clock generates a **1 Hz DCF77-pulse synchronisation pulse**, which can be used to synchronise further clocks (slaves).

Master operation means that the clock board is synchronised by the antenna signal. To do so an antenna or an antenna amplifier exit must be connected to the BNC connector of the board.

In case of **slave operation** the clock is synchronised with 1 Hz DCF77 pulses via a 9 pole Sub-D connector (see pin function in the appendix)

The service programme can be used to switch from master to slave operation or vice versa. The switching can also be implemented into own software.

The following commands switch the clock over to master operation:

no.	process	value (Hex)	port address (HEX)
1.	setting clock is master	80	2B0
2.	writing of status M/S	32	2B7

The following command combination switches the clock to slave operation:

no.	process	value (Hex)	port address (HEX)
1.	setting clock is slave	00	2B0
2.	writing of status M/S	32	2B7

8 Antenna Installation

8.1 Usable Types of Antennas

Only **hopf** antennas or multi antenna amplifiers should be connected to **hopf** radio clocks. This guarantees the best adaptation to the receiver.

Further antennas are available for the installation outdoors or in areas with particularly rough weather conditions or in locations with difficult reception situations:

- FG441700 outdoor antenna for pole installation with angled bracket
- FG441800 outdoor antenna for flat roof installation
- FG442000 outdoor antenna for pole installation without bracket
- FG443600 indoor antenna
- FG443700 outdoor antenna for all-round reception
- FG444000 indirect lightning protection
- FG444400 indirect lightning protection with 4x potential free antenna amplifier
- FG444600 4x potential free antenna amplifier

8.2 Alignment of the antenna

All active **hopf** antennas, except for the all-round antenna 4437, have an alignment characteristic. The antennas must therefore be aligned to the DCF77-transmitter. The location of the transmitter is Mainflingen near Frankfurt on the Main.

The indoor antenna 4436 is set at a right angle to the transmission direction of the transmitter, in case of the outdoor antennas the directional bar underneath the antenna housing must point to Frankfurt.

To align the antenna call up the programme **"SERVICE.EXE"** on the system disc (in mode 6035/6036 only).

The "alignment of the antenna " programme can be called up in the service menu to ensure that the antenna is installed correctly and that the DCF77-signal is not disturbed. This programme depicts the incoming DCF77-signal as an oscillogram on the screen.

Use key "A" to select the function "Alignment of the antenna"

After the start of the programme the amplification of the DCF77-signal is set again. Depending on the local field strength this process takes about 20-30 seconds.

The display shows the DCF77-signal oscillogram with a dipped signal on every second change (see picture one)

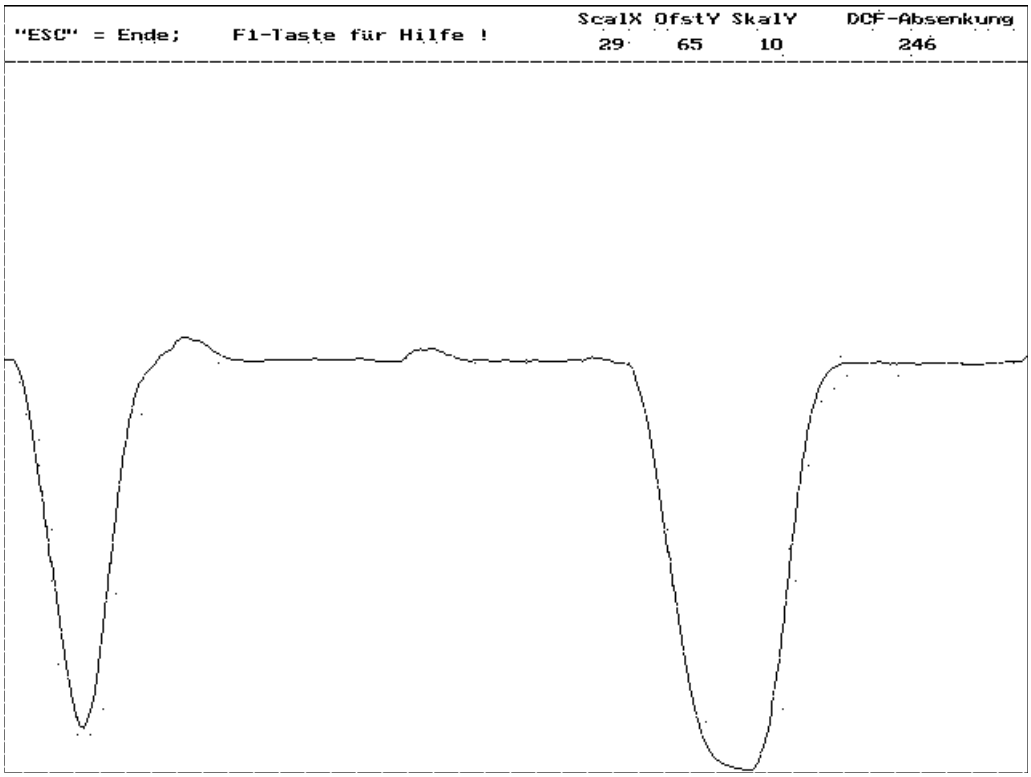
The newly set amplification is kept for length of the alignment programme.

If the antenna is slowly turned from this position the received field strength decreases if the antenna is positioned correctly. This is shown in a diminishing signal dip on the screen.

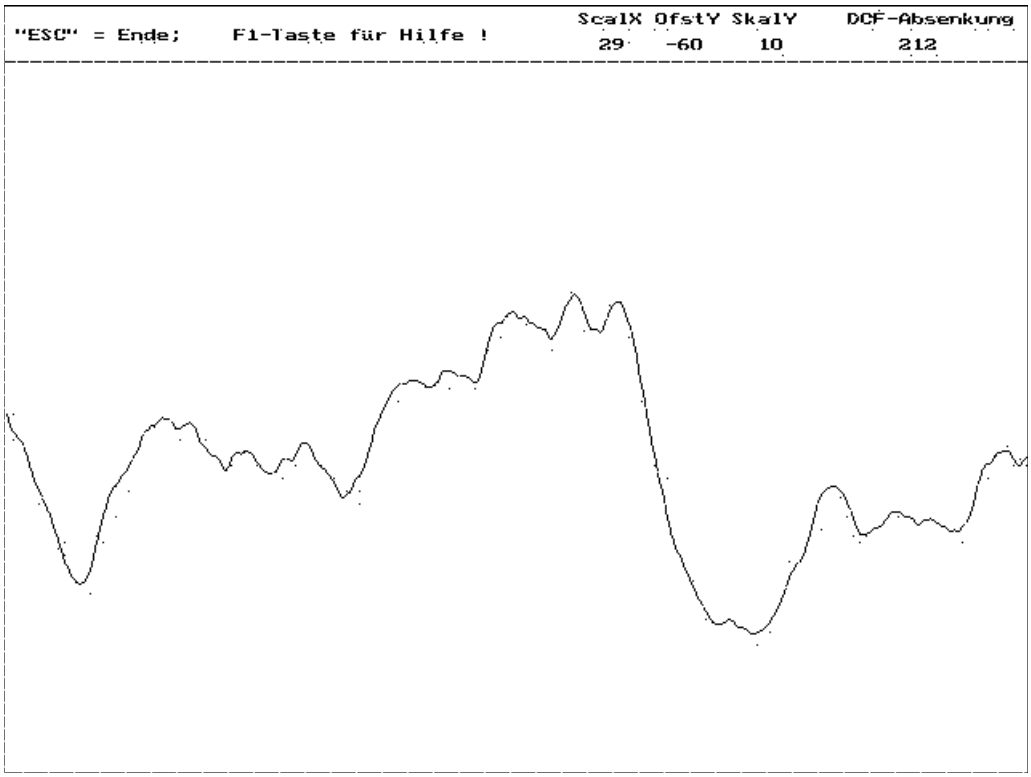
Turn the antenna until no DCF77-signal is left. From this minimum position the antenna is again turned by exactly 90° to the optimal position.

The programme can also be used to analyse the DCF77-signal.

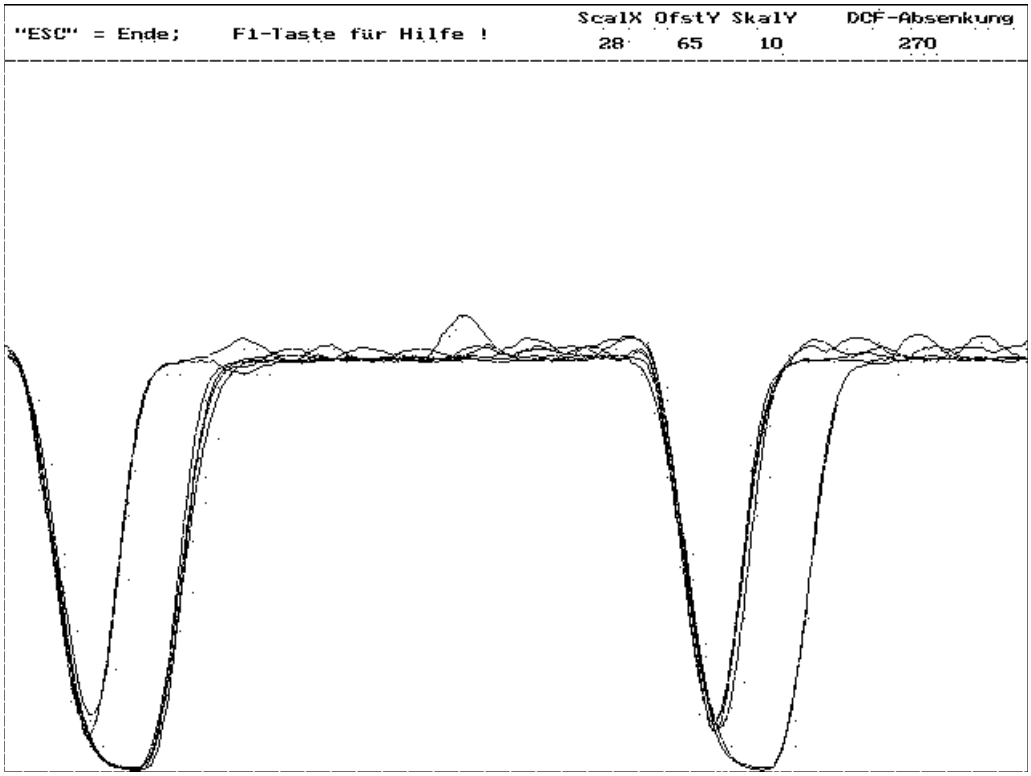
Picture 1 shows a noise-free reception. The signal lowering is easily recognisable as **naught** and **one** information. The DCF77-signal is not influenced by any source of interference.



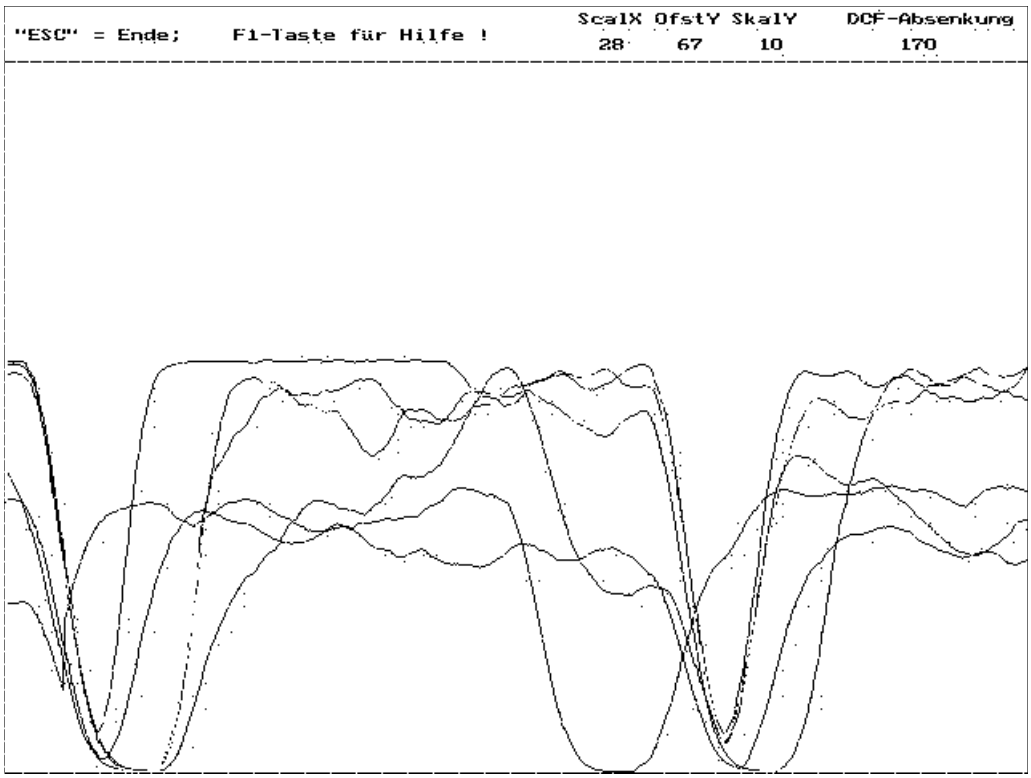
In picture 2 the antenna is near a monitor. The DCF77-signal is superimposed by an interfering frequency in the same frequency range. A **naught** and **a one** information is still recognisable in the left and right side of the picture. This does not suffice for the decoding of the signal.



Picture 3 shows a noise-free DCF77-signal with 6 passes. The **naughts** and **ones** of the DCF77-information are very obvious.

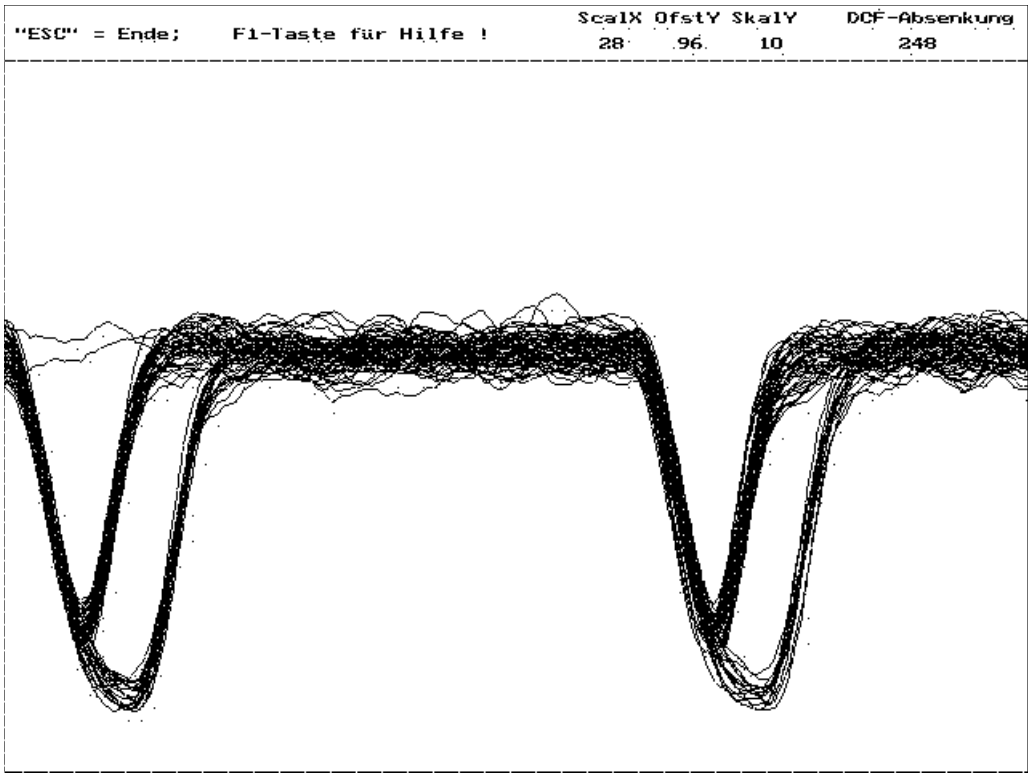


Picture 4 shows the same, but the antenna is again near a monitor. The decoding of the antenna position is not possible.



By means of the keys 0-9 the passes can be superimposed for easier evaluation. The keys 1-9 mean 1-9 passes, whereas entering naught superimposes all passes. In this mode all interferences are easily recognisable.

Picture 5 shows a two minute pulse sequence.



The cursor keys right and left can be used to scale the time axle. No more than three second markers should be shown on the screen during the signal analysis.

Please note : Screens and monitors interfere with the reception. The antenna should therefore be installed at a distance of at least 5-10m from the source of interference.

8.3 Indirect Lightning Protection

To avoid overvoltage caused by lightning we advise using an indirect lightning protection in case of the outdoor installation of the antenna.

9 Programming Help, Precautionary Measures and Source of Errors

In a multitasking situation the clock board should only be read by one process.

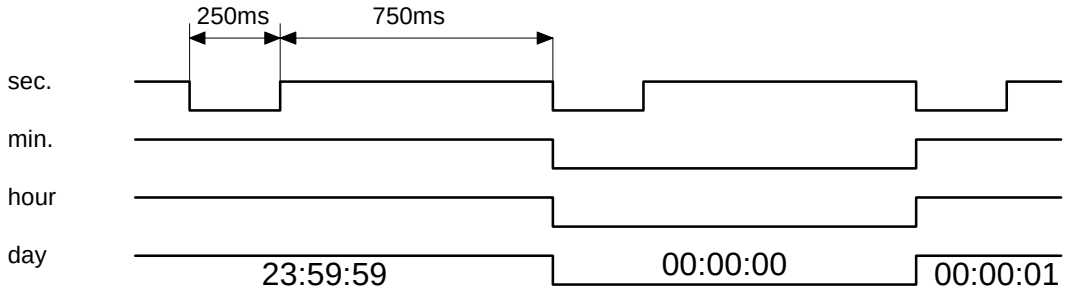
Data are exchanged between clock and computer via a dual-port RAM. It is therefore important to leave a resting period of ca. 1 ms between to accesses (reading one complete time information = 8 byte) for the updating of the clock data .

Computers with the choice whether to drive the ISA-bus synchronously or asynchronously , the bus must explicitly switched to asynchronous. The IOCHRDY signal is needed for a faultless data transmission.

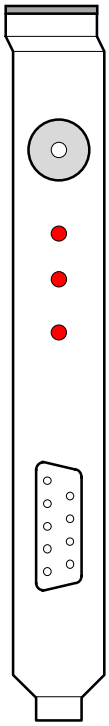
In case of interrupt operation accuses to the clock should occur only during the IRQ processing routine.

10 Pulse Output

Timing Diagram of the Signal on a 9-pole Sub-D-Connector



11 Description of the Front Panel of the Board



BNC-antenna connector

DCF77 pulse LED

status LED quartz

status LED radio

SUB-D connector 9 pole

pin	use	pin	use
1	day change	6	DCF77- pulse out
2	hour pulse	7	RS232 - RXD
3	minute pulse	8	RS232 - TXD
4	second pulse	9	DCF77- pulse in
5	GND		

12 Technical Data

operating voltage:	5V DC from the PC
current consumption	350 mA
receiver sensitivity:	< 100µV
perm. room temperature:	0 - 60°C
back-up clock accuracy:	± 25ppm at 25°C
quartz accuracy:	± 2ppm at DCF77 control
back-up clock operation	approx 3 days
accuracy of the internal second change at DCF77-reception:	± 2ms plus running time transmission-reception location

Please note : The ***hopf*** company withhold the right to hard and software alterations at any time!

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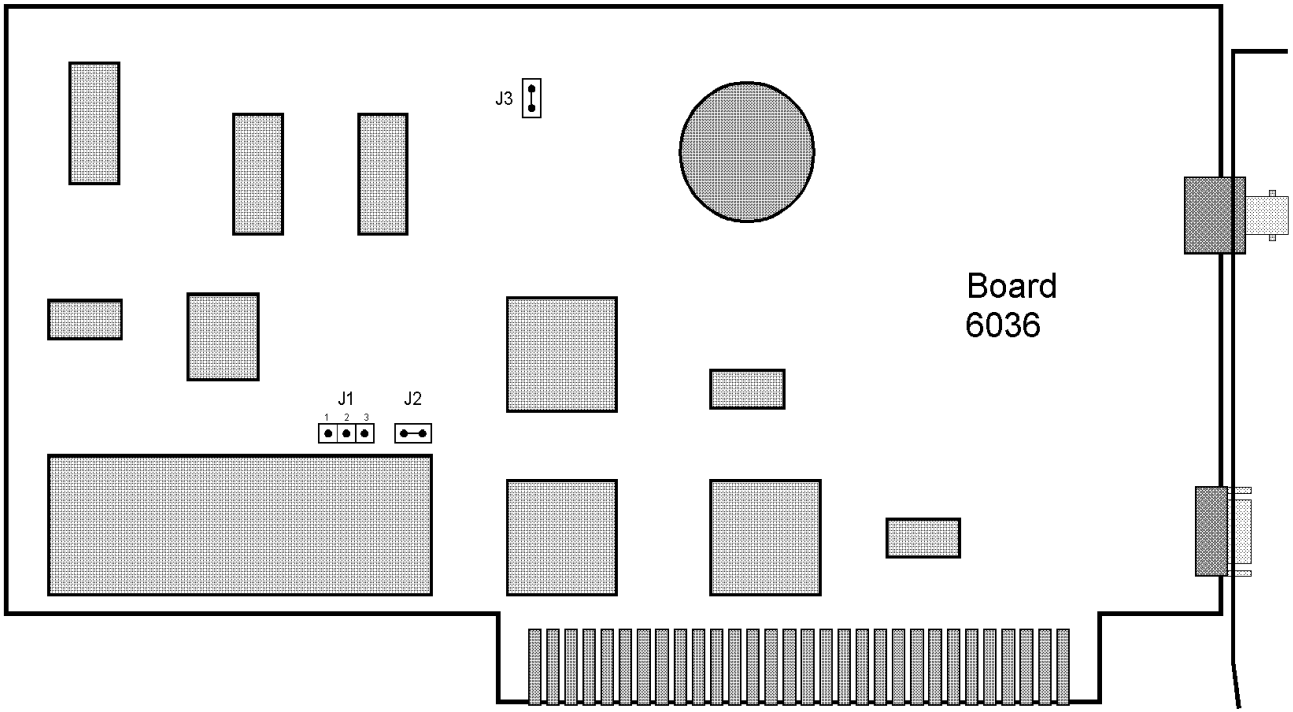
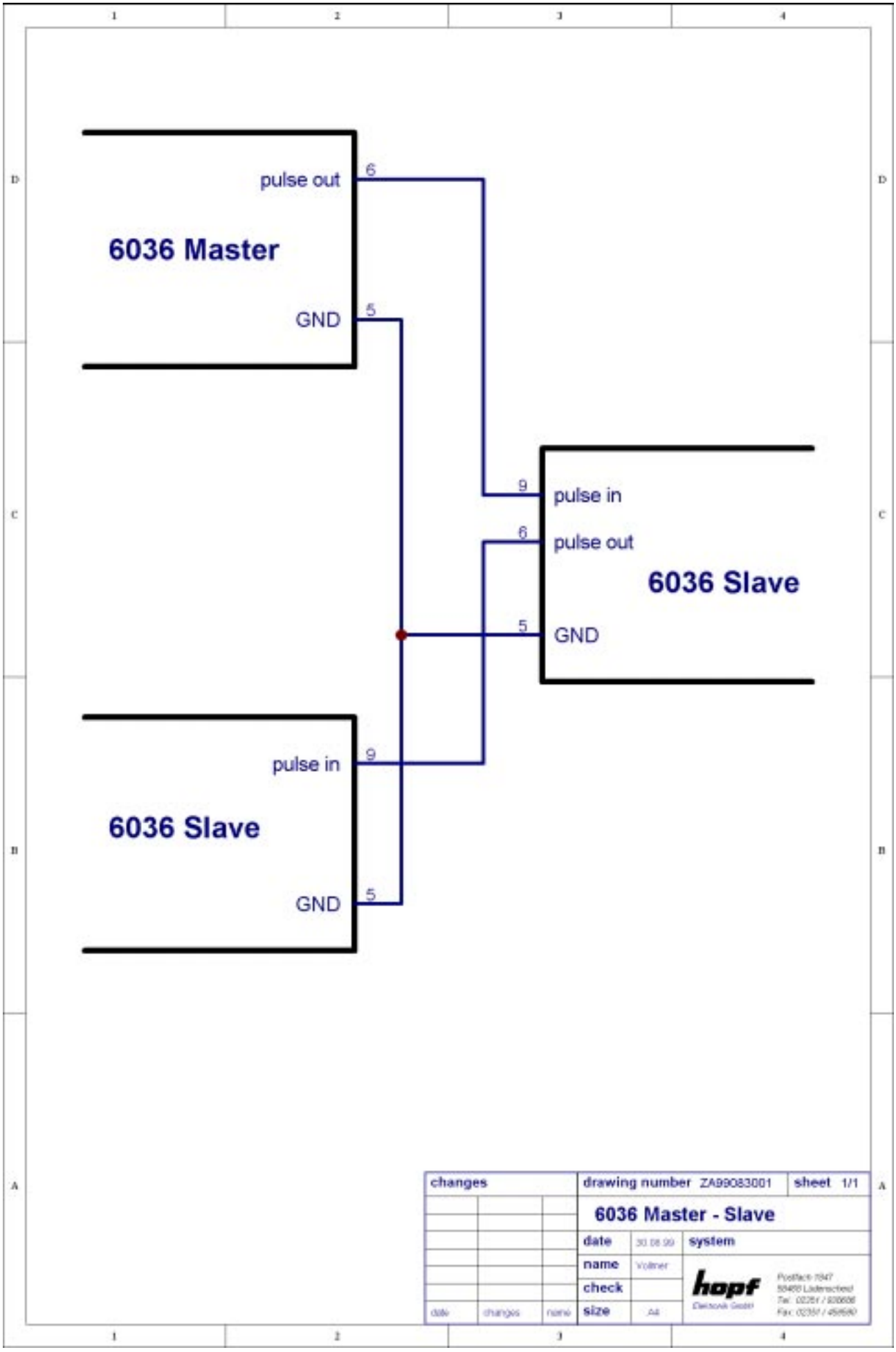
MsDos is a trade mark of the Microsoft Corporation



no. ZC97032501		page 1/1
	Board 6036	
	date 25.03.97	System
	name Vollmer	hopf Elektronik GmbH post box 1847 D-58468 Lüdenscheid fon: (02351) 938686 fax: (02351) 459590
	size A4	



changes			drawing number ZA99083001		sheet 1/1
			6036 Master - Slave		
			date	30.08.99	system
			name	Voltner	
			check		
date	changes	name	size	A4	

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